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Concept House  
Cardiff Road  
Newport  
South Wales  
NP10 8QQ

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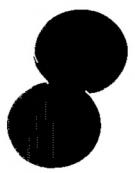
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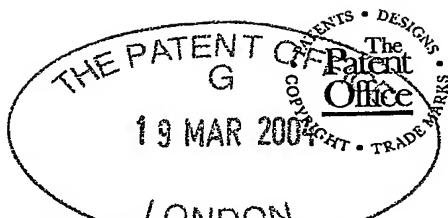
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1. Your reference

SAH03090GB

22MAR04 E882479-1 D02890

2. Patent application number

0406237.8

P01/7700 0.00-0406237.8 CHEQUE

19 MAR 2004

3. Full name, address and postcode of the or of each applicant (underline all surnames)

Matsushita Electric Industrial Co., Ltd.  
Matsushita IMP Building 19th Floor  
1-3-7 Shiromi Chuo-ku  
Osaka 540-6319  
JAPAN

Patents ADP number (if you know it)

59184 2007

If the applicant is a corporate body, give the country/state of its incorporation

JAPANESE

4. Title of the invention

Reprogramming a Non-Volatile Solid State Memory System

5. Name of your agent (if you have one)

Gill Jennings &amp; Every

"Address for service" in the United Kingdom to which all correspondence should be sent (including the postcode)

Broadgate House  
7 Eldon Street  
London  
EC2M 7LH

Patents ADP number (if you know it)

745002

6. Priority: Complete this section if you are declaring priority from one or more earlier patent applications, filed in the last 12 months.

Country

Priority application number  
(if you know it)Date of filing  
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7. Divisionals, etc: Complete this section only if this application is a divisional application or resulted from an entitlement dispute (see note f)

Number of earlier UK application  
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YES

Answer YES if:

- a) any applicant named in part 3 is not an inventor, or
- b) there is an inventor who is not named as an applicant, or
- c) any named applicant is a corporate body.

Otherwise answer NO (See note d)

# Patents Form 1/77

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Continuation sheets of this form

Description	6
Claim(s)	2
Abstract	1
Drawing(s)	4 + 4/4

10. If you are also filing any of the following, state how many against each item.

Priority documents

Translations of priority documents

Statement of inventorship and right to grant of a patent (Patents Form 7/77)

1

Request for a preliminary examination and search (Patents Form 9/77)

1

Request for a substantive examination (Patents Form 10/77)

NO

Any other documents (please specify)

11. I/We request the grant of a patent on the basis of this application.

For the applicant

Gill Jennings & Every

Signature

Date 19 March 2004

12. Name, daytime telephone number and e-mail address, if any, of person to contact in the United Kingdom

Stephen Haley  
020 7377 1377

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REPROGRAMMING A NON-VOLATILE SOLID STATE MEMORY SYSTEM

The present invention relates to the reprogramming of a part of a memory system that uses non-volatile memory and, particularly, to reprogramming a segmented memory system with in an embedded process system, for example flash memory.

In the past non-volatile flash memory has been treated as contiguous and, possibly continuous, storage area. Larger systems are known that comprise several flash memory chips which may not be adjoining in the memory space. When a change is required, therefore, the entire memory has to be reprogrammed. This is undesirable for a number of reasons. Firstly, as the amount of data to be transferred to an electronic device increases so the time taken for the reprogramming also increases. During this, increasing lengthy, reprogramming process the electric device is not in a usable state.

One approach that has been used to attempt to overcome these problems is to segment the memory. US-A-6295603 discloses a system incorporating a segmented controlled system. This invention seeks to overcome the problem of overwriting program code vital to the system boot-up process. The segmentation of the memory, along with the provisions of segment pointers, results in the memory area containing the program to be executed not being mapped onto a specific location within the memory. Manipulation of the address pointers is then used to minimise the chance of an inadvertent over writing of the boot-up code.

It is evident from this document that the segmentation of a solid state memory is a powerful tool. However, the system disclosed in US-A-6295603 makes only passive, rather than active use of segmentation to prevent unwanted overwriting of certain sections of a memory.

There are existing techniques that provide multiple "banks" of programme memory. The concept behind such systems is as follows: there are two banks of memory A and B. While bank A is executing the current version of the software, software A, bank B can be reprogrammed with new software, 5 software B. When the reprogramming is complete, the system is instructed using a soft reset to use the new software. Although this does facilitate reverting to software A in the event of a problem with software B, there is a requirement for double the memory required for software A alone. Furthermore, the redirection of the system to read from the other memory bank requires a soft 10 reset and this causes an interruption in service.

In other systems known in the art the new version of the program directly overwrites the old version. It is therefore not possible to regress to the earlier 15 version of the program if, for some reason, the reprogramming is unsuccessful and the new version of the program fails to operate correctly. This is very unsatisfactory as it renders a functional, if out of date, system initially unusable.

The present invention has been developed to overcome these problems.

20 According to the present invention there is provided a non-volatile memory system comprising:

non-volatile memory divided into a polarity of segments each segment having an address in an address space,

25 means for copying any one segment to be reprogrammed into a first RAM, the first RAM having a size at least equal to the segment size,

a second RAM for holding a reprogrammed code,

writing means for writing the reprogrammed code from the second RAM into the segment, and

30 control means arranged to enable execution of the program from the first RAM during the reprogramming.

The use of two RAM areas is advantageous because it means that there is no need for spare program memory and therefore the memory segments may be used to full capacity. Furthermore, there is no need for a permanent re-write of address as the address reverts to the original address once the re-write 5 has been completed.

The segments are preferably substantially equal in size. This minimises the size of RAM required as the RAM must be equal to the largest segment and if all of the segments are substantially the same size there will be no 10 redundancy in the RAM.

Preferably each segment contains some unused space. This space is preferably a small proportion of the segment. This space allows for the reprogrammed version to be slightly larger than the original version of the code. 15

The area of RAM to be used in this technique is equal in size to a single memory segment. This facilitates a 1:1 transfer between any non-volatile memory segment and the RAM and then subsequent 1:1 transfer of the modified segment in the RAM back into the original memory segment.

20 Furthermore, according to the present invention there is provided a method of reprogramming a non-volatile solid state memory system comprising a plurality of segments each segment having an address in an address space, two RAMs each at least equal in size to a single memory segment, and control 25 means capable of enabling the execution of the program from the first RAM during the reprogramming, the method comprising steps of:

copying at least one segment to be reprogrammed into the first RAM, diverting program execution to the first RAM,

holding a reprogrammed code in the second RAM,

30 writing the reprogrammed code from the second RAM into the at least one memory segment to be reprogrammed, and

reverting to the original address instructions for the segment.

The advantage of this method is that there is no requirement for spare memory segments and, furthermore, only a temporary divert of address is required.

Preferably there is so more provided a user interface for managing a method of reprogramming according to the present invention. The user interface is designed to guide the user through a reprogramming of a non-volatile solid state memory system comprising a plurality of memory segments each segment having an address in an address space, two RAMs each at least equal in size to a single memory segment, and control means capable of enabling the execution of the program from the first RAM during reprogramming, the user interface comprising:

a graphical representation of the embedded processor showing the contents of each segment, means for selecting the segment to be reprogrammed, and

means of implementing the method of reprogramming described above.

An example of the present invention will now be described with reference to the following figures in which:

Figures 1, 2 and 3 show the effective parts of processor system according to the present invention undergoing reprogramming.

Figure 4 is a schematic showing the connectivity of the embedded system of which the processor system of the present invention forms a part;

Figures 5a, b and c show the graphical user interface of the present invention during the reprogramming.

Each of Figures 1 to 3 shows the effective parts of a processing system 10 according to the present invention. The processing system 10 comprises a non-volatile memory 11 which, in this example, is divided into segments  $S_1$  to  $S_9$ . It will be appreciated that the invention can be applied to a memory with

other numbers of segments. Each of these segments  $S_1$  to  $S_9$  has a corresponding address in address space A1 to A9. The processor 10 also has two areas of RAM (RAM 1, RAM 2) that are the same size of one of the segments 11 and a memory management unit (MMU) or other logic to control 5 the switching of segments within the address space.

The process of reprogramming one segment, in this case segment  $S_4$ , is shown in figures 1, 2 and 3. Figure 1 represents the initial situation with each segment residing at an address having the same subscript as the segment 10 number. Segment  $S_4$  is to be modified. It is therefore copied into the RAM 1 and the memory management unit MMU instructs a divert to the version of  $S_4$  stored in the RAM 1. This situation is shown in Figure 2 where the RAM 1 contains the active version of  $S_4$  which has temporarily been given the address A4. The modified version of the program code intended for this segment is 15 copied into and held in RAM 2 where the required modifications are made to the code. The modified program code from RAM 2 is then reprogrammed into memory segment  $S_4$  and then the address divert is removed so that the processor executes the modified code now stored in segment  $S_4$  as shown in Figure 3.

20

Figure 4 shows the processor system 10 within the context of a computer system 1. The volatile memory 11 and RAM communicate with the processor 10 via a system bus 15 and address control logic 14 that processes the change of address information required during the reprogramming. The graphical user 25 interface appears on a display 16 to enable the user to instruct the reprogramming operation. This is convenient as the user must be able to control the process despite the fact that it is embedded deep within the computer system 1. Information from the processor 10 and address control logic 14 is supplied to the display 16 via the system bus 15 and display control logic 17. The user can use a mouse, touch screen or other suitable pointer to 30 input commands which are subsequently fed back to the processor 10 via

screen control logic 18. Alternatively the user can input commands through a keypad 19 that is connected, via keypad control logic 20, to the system bus 15.

Figures 5a, b and c show the graphical user interface at various stages 5 during the reprogramming process. The first step is to download the package to the system. This will result in the window shown in Figure 5a asking "Which Flash segment to update?" The user must then select a segment number "n" and proceed by either clicking the "OK" icon within the window, or giving a suitable command via the keyboard. The processor 10 then begins the 10 reprogramming process and the user is informed of the progress of the reprogramming by a window that progresses from that shown in Figure 5b to that shown in Figure 5c as the process proceeds. This window is for information only as the user cannot interrupt the process once it has been initiated.

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## CLAIMS

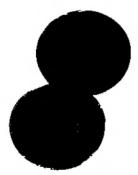
1. A non-volatile memory system comprising:  
non-volatile memory divided into a polarity of segments each segment  
5 having an address in an address space,  
means for copying any one segment to be reprogrammed into a first  
RAM, the first RAM having a size at least equal to the segment size,  
a second RAM for holding a reprogrammed code,  
writing means for writing the reprogrammed code from the second RAM  
10 into the at least one segment to be reprogrammed, and  
control means arranged to enable execution of the programme from the  
first RAM during the reprogramming.
2. The system according to claim 1, wherein the segments are substantially  
15 equal in size.
3. The system according to claim 1 or claim 2, wherein each segment  
contains some unused space.
- 20 4. The system according to any of claims 1 to 3, wherein the control means  
comprises internal logic components.
5. A method of reprogramming a non-volatile solid state memory system  
comprising a priority of segments each segment having an address in an  
25 address space, two RAMs each at least equal in size to a single memory  
segment, and control means capable of enabling the execution of the program  
from the first RAM during reprogramming, the method comprising steps of:  
copying at least one segment to be reprogrammed into the first RAM,  
diverting programme execution to the first RAM,  
30 holding a reprogrammed code in the second RAM,

writing the reprogrammed code from the second RAM into the at least one segment to be reprogrammed, and  
reverting to the original address instructions for the segment.

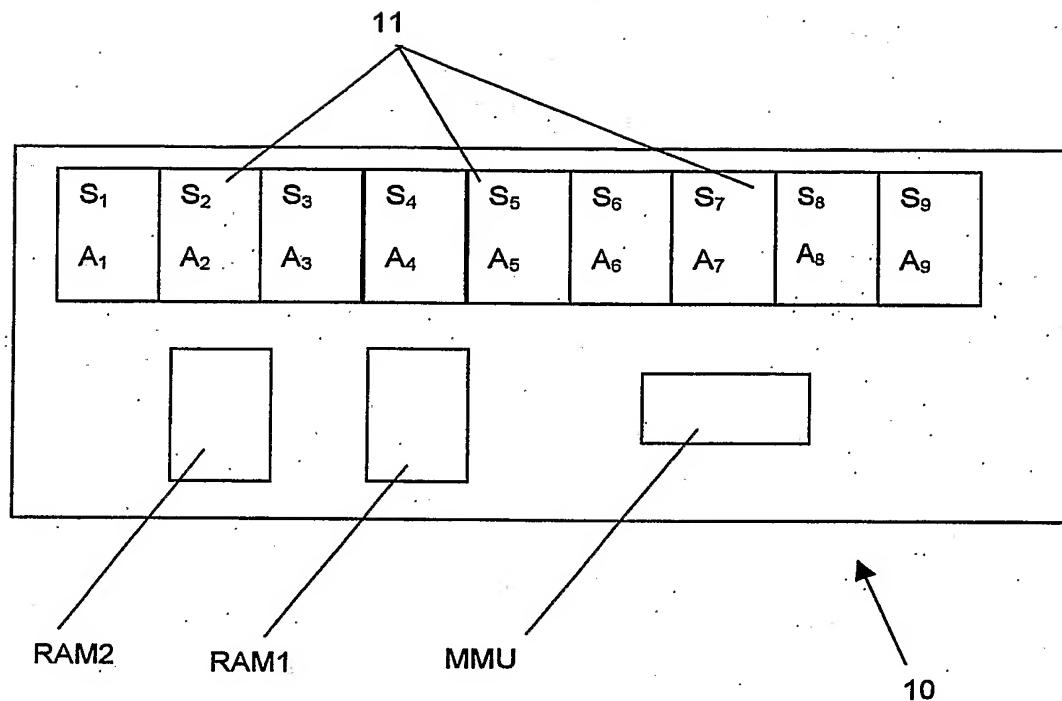
5     6. A user interface for guiding a user through a reprogramming of a non-volatile solid state memory system comprising a polarity of segments each segment having an address in an address space, two RAMs each at least equal in size to a single memory segment, and control means capable of enabling the execution of the programme from the first RAM during the reprogramming, the  
10    user interface comprising:  
          a graphical representation of the imbedded processor showing the contents of each segment,  
          means for selecting the segment to be reprogrammed, and  
          means of initiating the method of reprogramming according to any one  
15    of claims 5 to 7.

**ABSTRACT**

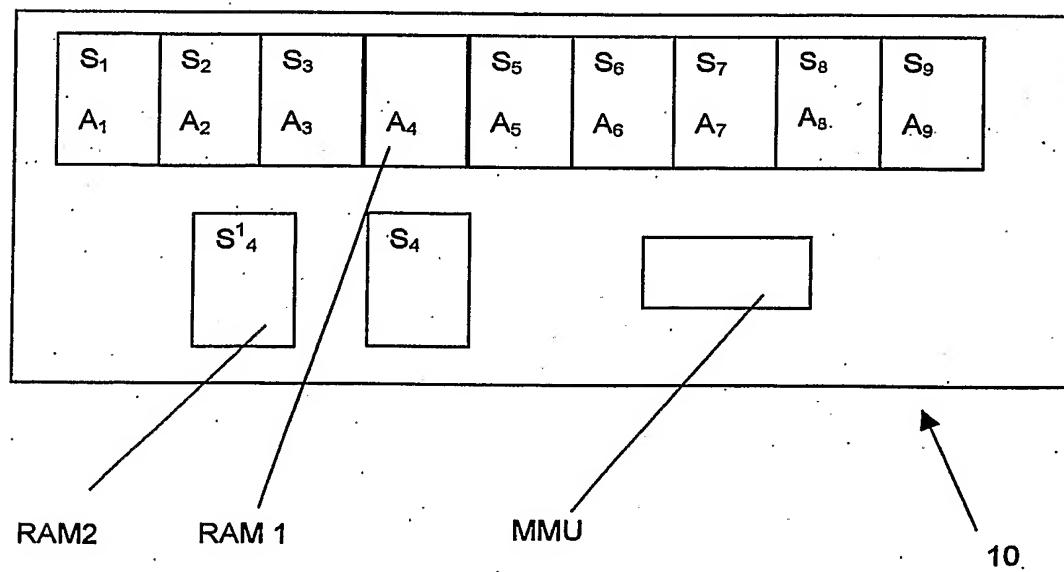
A non-volatile memory system is provided. The system comprises: non-volatile memory divided into a polarity of segments each segment having an address in an address space, means for copying any one segment to be reprogrammed into a first RAM, the first RAM having a size at least equal to the segment size. The system further comprises a second RAM for holding a reprogrammed code, writing means for writing the reprogrammed code from the second RAM into the at least one segment to be reprogrammed, and control means arranged to enable execution of the programme from the first RAM during the reprogramming.



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**Figure 1**



**Figure 2**



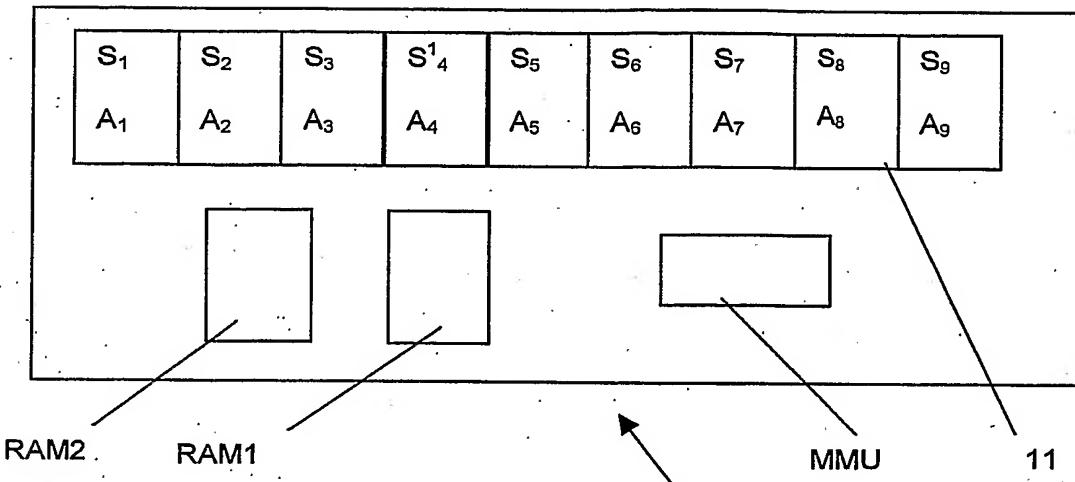


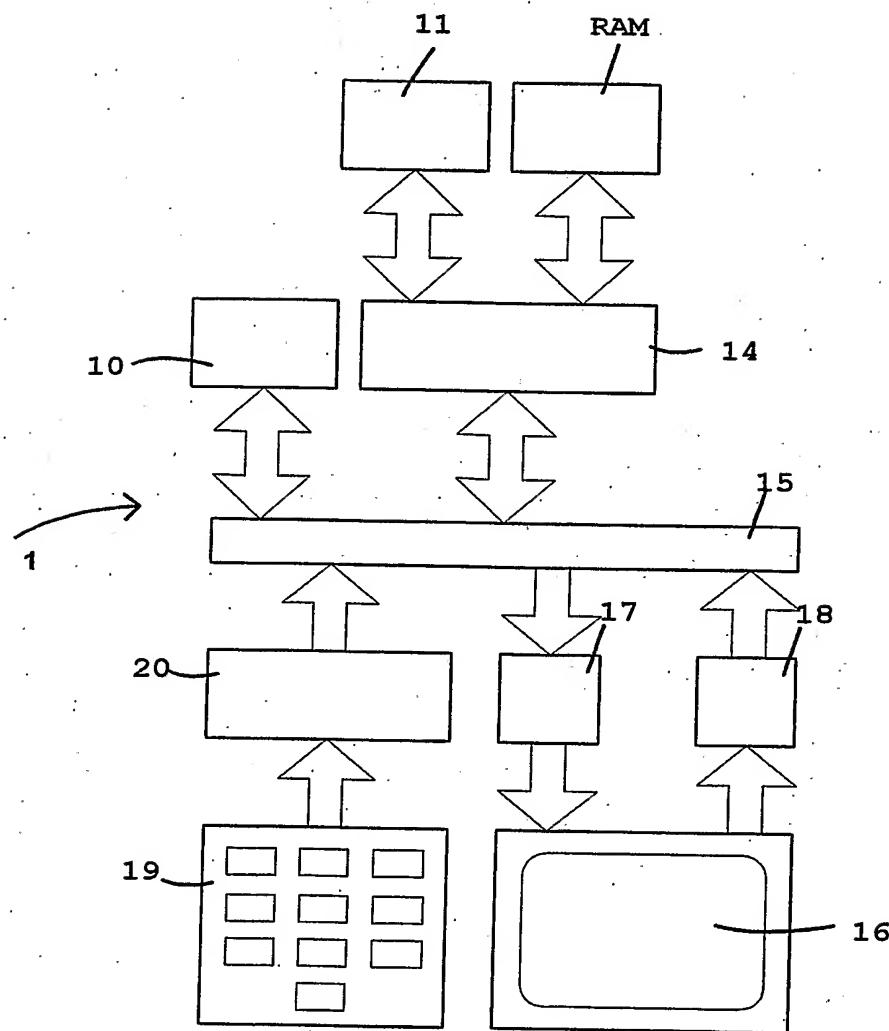
Figure 3

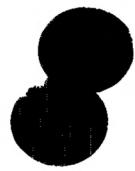
10

11



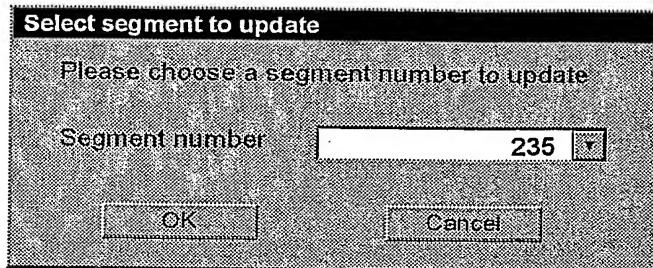
Figure 4



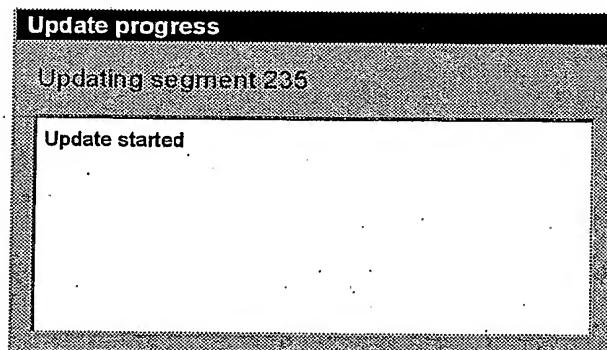


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**Figure 5A**



**Figure 5B**



**Figure 5C**

